PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10052255	01/23/2002	438	257	2829	GEYER

**APPLICANTS: Ebina Akihiro; Maruo Yutaka;

S.B.G.

**CONTINUING DATA VERIFIED:

NONE S.B.G.

** FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-021931(P) 01/30/2001 S.B.G.

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐

Foreign priority claimed	☒ yes ☐ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☒ yes ☐ no	111778
Verified and Acknowledged Examiners's intials		

TITLE : Method of manufacturing semiconductor integrated circuit device including nonvolatile semiconductor memory devices

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED
	Assistant Examiner	Total Claims / Print Claim for O.G.
ISSUE FEE		DRAWING
Amount Due / Date Paid		Sheets Dwg. / Fig. for O.G. / Print Fig.
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner
	PREPARED FOR ISSUE	

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM (Attached in pocket on right flap)